REMARKS

The Examiner's Action mailed on June 15, 2004 has been received and its contents carefully considered. In this Amendment, the applicant has amended claims 3, 10, and 12 and cancelled 1, 2, 5, 7 - 9, 11, 13 - 16, 22 – 25. New claims 26 - 28 have been added to further protect the invention. Reexamination and reconsideration of the amended application respectfully is requested. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner rejected claims 10, 12 and 17-21 under 35 USC 103(a) as being unpatentable over *Sekine et al.* in view of *Admission* or *Frye et al.* The rejection of claims 17-21 is respectfully traversed. Claims 10 and 12 have been amended, and it is submitted that the rejection is inapplicable to the amended claims.

Claim 10 has been amended to clarify that the structure defined in the claim is on a wafer level basis so that a plurality of separate chip-on-chip devices can be produced therefrom. That is, claim 10 has been amended to clarify that the semiconductor device of the invention includes a plurality of first semiconductor chips bonded onto a surface of a solid device. The solid device includes a plurality of second semiconductor chips, respectively disposed below the first semiconductor chips such that each first semiconductor chip and the second semiconductor chip therebelow define a respective chip-on-chip structure.

The references alone or in combination nowhere show or suggest such a structure as defined in amended claim 1. As already discussed in response to a previous Action, and acknowledged by the Examiner, *Sekine et al.* clearly do not teach or even suggest a chip-on-

chip, but a multi-chip module. And while *Admission* and *Frye et al.* disclose chip-on-chip structures, neither show or suggest to bond a plurality of first semiconductor chips onto a surface of a solid device that includes a plurality of second semiconductor chips, respectively disposed below the first semiconductor chips such that each first semiconductor chip and the second semiconductor chip therebelow define a respective chip-on-chip structure, whereby a plurality of separate chip-on-chip devices are formed on a wafer level basis, so that individual separate chip-on-chip devices can be produced therefrom. A person or ordinary skill in the art therefore would not combine the teachings of either of these secondary references with those of the primary reference, since the secondary references say nothing about and are unrelated to a chip-on-chip structure or its formation on a wafer level.

Thus, for the above reasons, it is submitted that a person of ordinary skill in the art is provided with no teachings from which it would be obvious to combine these references to produced the claimed invention. Claim 10 and claim 12 depending therefrom are deemed clearly to be patentable over *Sekine et al.* in view of *Admission* or *Frye et al*, and the rejection accordingly should be withdrawn.

Claim 17 is directed to a method for manufacturing a semiconductor device that terminates with taking out individual pieces of chip-on-chip type semiconductor devices by cutting the semiconductor substrate along predetermined cutting lines. Thus, again, the claimed invention is directed to the creation of chip-on-chip structures on a wafer level basis, which is followed by cutting the semiconductor substrate along predetermined cutting lines to produce the individual structures. No combination of the cited references shows or suggests such a

method. Indeed, the very idea of producing individual chip-on-chip structures by forming first chips on second chips defined by on respective active surfaces of a semiconductor substrate, and then cutting them apart, is nowhere shown or suggested. Without this idea, the claimed invention cannot be obtained. Therefore, claim 17, and claims 18-21 depending therefrom are deemed clearly to be patentable over the cited references and the rejection accordingly should be withdrawn.

The Examiner also rejected claims 10 and 12 under 35 USC 103(a) as being unpatentable over *Egawa* in view of *Admission* or *Frye et al.* The rejection respectfully is traversed for reasons similar to those presented against the rejection of these claims over *Sekine et al.* in view of *Admission* or *Frye et al.* That is, *Egawa* clearly and admittedly by the Examiner, does not teach or even suggest a chip-on-chip, and neither *Admission* nor *Frye et al.* say anything about and are unrelated to a chip-on-chip structure or its formation, on a wafer level. A person or ordinary skill in the art therefore would not combine the teachings of either of these references with those of the primary reference.

Thus, for the above reasons, it is submitted that a person of ordinary skill in the art is provided with no teachings from which it would be obvious to combine these references to produced the claimed invention. Claim 10 and claim 12 depending therefrom therefore are deemed clearly to be patentable over *Egawa* in view of *Admission* or *Frye et al*, and the rejection accordingly should be withdrawn.

The Examiner also rejected claims 3, 4 and 6 under 35 USC 103(a) as being unpatentable over *Sekine et al.* in view of *Fukasawa et al.* and *Ichikawa.* Claim 3 has been

amended, and it is submitted that the rejection is inapplicable to amended claim 3 and claims 4 and 6 depending therefrom.

Claim 3 has been amended to clarify that the method of manufacturing a semiconductor device according to the invention includes

(i) forming a back side resin layer on a back side of a semiconductor substrate so that a surface resin layer and the back side resin layer have substantially the same thickness respectively,

(ii) by polishing or grinding the surface resin layer, a surface grinding step that exposes from the surface resin layer projection electrodes that have been formed on a substrate surface,

(iii) bracing the substrate with the back side resin layer while performing the surface grinding step so as to inhibit warpage of the substrate, and

(iv) after the surface grinding step, performing a back side grinding step of thinning the semiconductor substrate by

(a) removing the back side resin layer, through polishing or grinding, from the semiconductor substrate provided with the surface resin layer and the back side resin layer, and

(b) further polishing or grinding the back side of the semiconductor substrate from which the back side resin layer has been removed.

An aspect of the invention is that the front grinding step is performed after the back side grinding. The Examiner acknowledges that none of the cited references teaches this feature. However, the Examiner has taken a position that the ordering of these steps is not a patentable

feature, arguing that "[t]he transposition of process steps where the process are substantially identical or equivalent in terms of function, manner and result has been held to be [sic]not patentably distinguish the processes" citing *Ex Parte Rubin* 128 USPQ 159.

The Examiner has applied this case on the basis of his opinion that "applicant's specification merely teaches a preference of order without demonstrating an unexpected result and the instant specification also teaches the sequence of the steps in not critical because the steps can be interchanged."

The applicant would strenuously disagree with the Examiner's application of law to the facts of this case. The fact that the front grinding step can be performed before the back side grinding does not make the ordering noncritical to the invention. We believe that the specification makes clear that the ordering is critical to obtain the benefit discussed on page 30. The fact that according to a broader definition of the invention, the steps could be reversed, does not mean the ordering is not critical to the more narrowly defined invention in which the ordering is specified. Thus, the **ordering is critical** to the claimed invention. It also is clear that the function, manner and result are not the same if the steps are reversed because the back side resin layer performs a function while the front side layer is being ground, that it clearly cannot perform if it has already been ground in advance. And of course the result is different in terms of layer uniformity depending on the order of the steps.

The Examiner also takes the position that the specification does not demonstrate that the result of the invention is unexpected. However, we would point out it is not up to the applicant

to demonstrate that the result is unexpected. That the result is unexpected can be inferred from the advantage and the fact that it has not been shown to be known in the prior art.

The Examiner states that the order of grinding is not critical because warping may not occur even if the order of grinding is reversed. However, warping is prone to occur if the back side is ground first.

This may be explained as follows: The applicants have noted as to the ordering of the front surface grinding and the back surface grinding, that the warpage of the substrate does not occur during the surface grinding step because, before the surface grinding step, the surface resin layer and back side resin layer have substantially the same thickness. During the front surface grinding step, the substrate may be placed, for example, on a surface of a vacuum chuck and the front surface thereof pressed by the surface of the grinding head of a grinder. Therefore, the warpage of the substrate is unlikely to occur during the front surface grinding step. If there is a certain time between the front surface grinding step and the back surface grinding step, then the warpage of the substrate occurs during such time period. In this case, at the initial stage of the back side grinding step, this surface of the back side resin layer may not uniformly contact with the grinding head of a grinder, so that uniform polishing or grinding or the back side resin layer may become difficult.

If the back side grinding step is performed first and the front surface grinding step is performed thereafter, then the substrate may have warpage before the front surface grinding step. Therefore, at least during the initial stage of the front surface grinding step, the grinding head of a grinder may not uniformly contact the surface resin layer, resulting in non-uniform

thickness of the surface resin layer. This in turn results in non-uniform heights of projection electrodes on the surface of the substrate.

To emphasize the function of the elements, claim 3 has been amended to make explicit that by grinding the back side last, the substrate is braced with the back side resin layer during the surface grinding step to inhibit warpage of the substrate.

A further point we would make is that choosing to conduct the back side or front side grinding first is not a simple matter of design choice. It must be kept in mind in this regard that a manufacturer seeking to improve on the method of the primary reference, *Sekine et al.,* has first to make many choices that result in several other claimed steps before even getting to the issue of order of grinding, as described, for example, by the Examiner on pages 6-8 of the Action. It would therefore be a gross oversimplification to say that to obtain the invention, a skilled person need only select between two orders of grinding. Moreover, we would note that while the specification describes two possible orders of grinding as being possible, neither the present specification nor the prior art anywhere states or implies that grinding the front surface first and the back afterward is an alternative known to those skilled in the art.

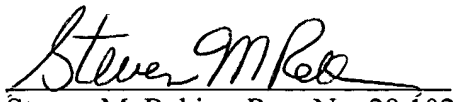
In view of the above, it is deemed to be clear that claim 3 and claims 4 and 6 depending therefrom clearly are patentable over the cited references. The rejection accordingly should be withdrawn.

Therefore, based on the above, it is submitted that this application is in condition for allowance. Such a Notice, with allowed claims 3, 4, 6, 10, 12 and 17-21, and 26 - 28, earnestly is solicited.

Should the Examiner feel that a conference would help to expedite the prosecution of the application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such a conference. Should any additional fee be required, or if no payment is attached, please charge the same to our Deposit Account No. 18-0002 and advise us accordingly.

Respectfully submitted,

September 15, 2004
Date



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